#6 8/10/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

TAKENO

Attorney Docket No: 107242-00024

Application No. 09/926,202

Group Art Unit: 1765

Filed: September 24, 2001

Examiner: M. Anderson

For: MANUFACTURING PROCESS FOR SILICON EPITAXIAL WAFER

AMENDMENT AND RESPONSE UNDER 37 C.F.R. § 1.111

Commissioner for Patents
Washington, D.C. 20231

August 7, 2002

Sir:

In reply to the Office Action dated May 8, 2002, please consider the following remarks during the prosecution of the above-identified application:

REMARKS

The Office Action dated May 8, 2002 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Accordingly, claims 6-21 are pending in this application and are submitted for consideration.

Claims 6-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wijaranakula (U.S. Patent No. 5,611,855) in view of Wolf et al. *Silicon Processing for the VLSI Era* (Wolf). In making this rejection, the Office Action took the position that Wijaranakula discloses all the elements of the claimed invention, except for disclosing the deposition temperature of the epitaxial layer or the oxygen concentration in units of atoms/cm^3. However, Applicant respectfully submits that claims 6-21 recite subject matter that is neither disclosed nor suggested in any combination of Wijaranakula or Wolf.